**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

ATTY.'S DOCKET: RINDNER=1

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| In re Application of: | ) | Art Unit: 2171 |
| | ) | |
| Yossi RINDNER | ) | Examiner: |
| | ) | |
| Appln. No.: 10/091,393 | ) | Washington, D.C. |
| | ) | |
| Date Filed: March 7, 2002 | ) | Confirmation No. 8666 |
| | ) | |
| For: SYSTEM AND METHOD FOR AUTOMATION OF ASIC SYNTHESIS FLOW | ) | April 19, 2002 |

**PRELIMINARY AMENDMENT**



Honorable Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination, please make the following changes to the above-referenced application:

**IN THE SPECIFICATION**

Please amend page 1, lines 20-25 of the specification as follows (attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached version is captioned "Version with Markings to Show Changes Made"):

ASICs are comprised of memory elements (registers) and arithmetic elements (gates). The registers and gates are cascaded, such that when the data memorized by a register is

processed by the following gate, the result is memorized again by the following register. The ASIC designer determines which gates should reside between the registers, how many of them to use, and their order - commonly referred to as RTL (Register Transfer Level) design.

**IN THE CLAIMS**

In view of the fact that the claims in the application as filed are misnumbered, applicant requests a renumbering of the claims as indicated below:

Please amend the claims by rewriting originally misnumbered claims 4-16 in amended form as follows (attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached version is captioned "Version with Markings to Show Changes Made"):

**3.** (Amended) The method according to Claim 1 further comprising:

**(vi)** obtaining third script files from an external source, and

**(vii)** feeding said third script files to the second stage for processing the output data in accordance with information contained in the third script files.

4. (Amended) The method according to Claim 1 including using a pre-prepared template for automatically generating the first script files.

5. (Amended) An apparatus for interfacing between first and second successive stages of an ASIC synthesis tool, said apparatus comprising:

a processor,

a plurality of selectors coupled to the processor and each corresponding to a tool for performing a stage in an ASIC design, and

a memory coupled to the processor and storing therein respective script files relating to each of said selectors;

said processor being responsive to selection of at least one of the selectors for accessing the memory and executing commands associated therewith.

6. (Amended) The apparatus according to Claim 5, wherein the commands executed by the processor are extracted from the respective script file relating to each of said selected selectors.

7. (Amended) The apparatus according to Claim 6, wherein the script file relating to each of said selected selectors is automatically generated.

**8.** (Amended) The apparatus according to Claim 6, wherein the script file relating to each of said selected selectors is automatically generated according to a pre-prepared template.

**9.** (Amended) The apparatus according to Claim 8, wherein the pre-prepared template is part of the selected selector.

**10.** (Amended) The apparatus according to Claim 8, wherein the pre-prepared template is a pre-prepared external file.

**11.** (Amended) The apparatus according to Claim 10, wherein the pre-prepared external template file is an XML file.

**12.** (Amended) The apparatus according to Claim 5, wherein the commands executed by the processor are parts of each of said selected selectors.

**13.** (Amended) The apparatus according to Claim 5, wherein at least some of said selectors are operable via a graphical user interface.

**14.** (Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for

interfacing between first and second successive stages of an ASIC synthesis tool, said method comprising:

**(i)** receiving output data at an output of the first stage,

**(ii)** automatically generating first script files, and

**(iii)** feeding said output data and said first script files to the second stage for processing the output data in accordance with information contained in the first script files.

**15.** (Amended) A computer program product comprising a computer useable medium having computer readable program code embodied therein for interfacing between first and second successive stages of an ASIC synthesis tool, said computer program product comprising:

computer readable program code for causing the computer to receive output data at an output of the first stage,

computer readable program code for causing the computer to automatically generate first script files, and

computer readable program code for causing the computer to feed said output data and said first script files to the second stage for processing the output data in

accordance with information contained in the first script files.

**REMARKS**

A review of the application shows that the application as filed contains no claim 3 and that claims 7, 8, and 12 as originally filed are improperly dependent, i.e. depend on themselves. The above amendments correct these errors.

Such amendments are not "narrowing" amendments, as the scope of the claims has not been changed. No limitations have been added and none are intended.

Applicant respectfully awaits the results of a first examination on the merits.

Respectfully submitted,

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Version with Markings to Show Changes Made

**In the Specification**

Page 1, lines 20-25:

~~ASIC~~ ASICs are comprised of memory elements (registers) and arithmetic elements (gates). The registers and gates are cascaded, such that when the data memorized by a register is processed by the following gate, the result is memorized again by the following register. The ASIC designer determines which gates should reside between the registers, how many of them to use, and their order - commonly referred to as RTL (Register Transfer Level) design.

**In the Claims**

4~~2~~3. (Amended) The method according to Claim ~~21~~ further comprising:

**(vi)** obtaining third script files from an external source, and

**(vii)** feeding said third script files to the second stage for processing the output data in accordance with information contained in the third script files.

5~~4~~. (Amended) The method according to Claim 1 including using a pre-prepared template for automatically generating the ~~third~~ first script files.

~~5~~5. (Amended) An apparatus for interfacing between first and second successive stages of an ASIC synthesis tool, said apparatus comprising:

a processor,

a plurality of selectors coupled to the processor and each corresponding to a tool for performing a stage in an ASIC design, and

a memory coupled to the processor and storing therein respective ~~command~~ script files relating to each of said selectors;

said processor being responsive to selection of at least one of the selectors for accessing the memory and executing commands associated therewith.

~~7~~6. (Amended) The apparatus according to Claim ~~7~~5, wherein the commands executed by the processor are extracted from the respective ~~command~~ script file relating to each of said selected selectors.

~~8~~7. (Amended) The apparatus according to Claim ~~8~~6, wherein the ~~command~~ script file relating to each of said selected selectors is automatically generated.

~~9~~8. (Amended) The apparatus according to Claim ~~8~~6, wherein the ~~command~~ script file relating to each of said selected selectors is automatically generated according to a pre-prepared template.

~~10~~9. (Amended) The apparatus according to Claim ~~9~~8, wherein the pre-prepared template is part of the selected selector.

~~11~~10. (Amended) The apparatus according to Claim ~~10~~8, wherein the pre-prepared template is a pre-prepared external file.

~~12~~11. (Amended) The apparatus according to Claim ~~12~~10, wherein the pre-prepared external template file is an XML file.

~~13~~12. (Amended) The apparatus according to Claim ~~7~~5, wherein the commands executed by the processor are parts of each of said selected selectors.

~~14~~13. (Amended) The apparatus according to Claim ~~7~~5, wherein at least some of said selectors are operable via a graphical user interface.

~~15~~14. (Amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for interfacing between first and second successive stages of an ASIC synthesis tool, said method comprising:

**(i)** receiving output data at an output of the first stage,

**(ii)** automatically generating first script files, and

**(iii)** feeding said output data and said first script files to the second stage for processing the output data in accordance with information contained in the first script files.

~~16~~15. (Amended) A computer program product comprising a computer useable medium having computer readable program code embodied therein for interfacing between first and second successive stages of an ASIC synthesis tool, said computer program product comprising:

computer readable program code for causing the computer to receive output data at an output of the first stage,

computer readable program code for causing the computer to automatically generate first script files, and

computer readable program code for causing the computer to feed said output data and said first script files to the second stage for processing the output data in accordance with information contained in the first script files.